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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,266	01/22/2002	Ki-won Choi	9898-208	6747

7590 07/11/2003

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EXAMINER
VU, QUANG D

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/055,266	CHOI, KI-WON	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on 04/22/03* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,12-16,26 and 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12-16,26 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities: In lines 10-12, page 6, the phrase "...the substrate is a single layer, a double layer, or a multi layer substrate" is unclear. Figure 6 shows that the substrate (100) includes the substrate and printed circuit pattern (106). Is it being referred to a single layer or a double layer substrate? Appropriate correction is required.

Claim Objections

Claim 27 is objected to because of the following informalities: Claim 17 has been cancel. It is unclear why claim 27 depends on claim 17. Appropriate correction is required.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3-4, 6-10, 16, 26 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,448,664 to Tay et al.

Regarding claim 1, Tay et al. (figures 9A-B) teach a semiconductor package comprising:

a substrate (72) including a redundant bond finger (76), an added bond finger (a pad formed along the first inner rectangle) connected to a redundant solder ball (80);

a semiconductor chip (92) having an added bond pad (106) attached to the substrate (72);

a normal wire bonding unit coupled between the added bond pad (106) and the redundant bond finger (76).

an added wire bonding unit (a line connecting [76] and the added bond finger) coupled between the redundant bond finger (76) and the added bond finger (a pad formed along the first inner rectangle).

wherein the added bond pad (106) is electrically connected to the redundant solder ball (80) via the redundant bond finger (76) and the added bond finger (a pad formed along the first inner rectangle).

Regarding claim 3, Tay et al. inherently teaches a solder ball connected to the redundant solder ball pad (80).

Regarding claim 4, Tay et al. teach the substrate (72) is a single layer substrate. It is inherent to have printed circuit patterns because the printed circuit patterns are used to connect the chip and the solder balls.

Regarding claim 6, it is inherent that a solder mask is not formed on the added bond finger because Tay et al. never discloses a solder mask.

Regarding claim 7, Tay et al. teach the added wire bonding unit (a line connecting [76] and the added bond finger) is formed over the substrate (72).

Regarding claim 8, Tay et al. teach the added wire bonding unit (a line connecting [76] and the added bond finger) is formed on an outer region of the substrate (72) on which the semiconductor chip (92) is mounted.

Regarding claim 9, Tay et al. teach the added wire bonding unit (a line connecting [76] and the added bond finger) is one unit.

Regarding claim 10, Tay et al. teach the semiconductor chip (92) is attached to the substrate (72) using an adhesive (90).

Regarding claim 13, Tay et al. (figures 9A-B) teach a semiconductor package comprising:

a substrate (72) including a first printed circuit pattern (a printed circuit pattern is formed between the redundant bond finger [76] and the added bond finger (a pad formed along the first inner rectangle)) connected to a redundant bond finger (76) and a second printed circuit pattern (a printed circuit pattern is formed between the added bond finger and the solder ball [80] along the edge of the substrate) connected to a redundant solder ball (80);

a semiconductor chip (92) attached to the substrate (72); and

an added wire bonding unit (a line connecting [76] and the added bond finger) coupled between the first printed circuit pattern (a printed circuit pattern is formed between the redundant bond finger [76] and the added bond finger) to the second printed circuit pattern (a printed circuit pattern formed between the added bond finger and the solder ball [80] along the edge of the substrate) to electrically connect the redundant bond finger (76) to the redundant solder ball (80).

Regarding claim 16, Tay et al. inherently teach the first printed circuit pattern (a printed circuit pattern is formed between the redundant bond finger [76] and the added bond finger) and a second printed circuit pattern (a printed circuit pattern formed between the added bond finger

and the solder ball [80] along the edge of the substrate) each have a width that enables wire bonding to be performed thereon.

Regarding claim 26, Tay et al. (figures 9A-B) teach a semiconductor package comprising:

a semiconductor chip (92) having an added bond pad (106);

a substrate (72) having a redundant bond finger (76) and an added bond finger (a pad formed along the first inner rectangle) connected to a redundant solder ball (80);

a normal wire bonding unit coupled between the added bond pad (106) and the redundant bond finger (76); and

an added wire bonding unit (a line connecting [76] and the added bond finger) coupled between the redundant bond finger (76) and the added bond finger (a pad formed along the first inner rectangle) such that the added bond pad (106) is electrically connected to the redundant solder ball (80) via the redundant bond finger (76) and the added bond finger (a pad formed along the first inner rectangle).

Regarding claim 27, Tay et al. (figures 9A-B) teach the added bond finger (a pad formed along the first inner rectangle) is not directly connected to the added bond pad (106).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 5, 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,448,664 to Tay et al. in view of Admitted Prior Art.

Regarding claim 2, Tay et al. differ from the claimed invention by not showing an encapsulant for encapsulating the semiconductor chip, the normal and added wire bonding units. However, Admitted Prior Art (figures 1-2) teaches an encapsulant (7). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate an encapsulant of Admitted Prior Art into the device of Tay et al. because it protects device from the external environment. The combined device shows that an encapsulant for encapsulating the semiconductor chip, the normal and added wire bonding units.

Regarding claim 5, Tay et al. differ from the claimed invention by not showing the substrate is a double layer substrate or a multi layer substrate. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the substrate is a double layer substrate or a multi-layer substrate because it depends on the size of the package.

Regarding claim 12, Tay et al. differ from the claimed invention by not showing the added bond finger has the same pad shape as that of the redundant bond finger. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the added bond finger has the same pad shape as that of the redundant bond finger because it depends on the size of the substrate.

Regarding claim 14, Tay et al. differ from the claimed invention by not showing an encapsulant for encapsulating the semiconductor chip and the added wire bonding units. However, Admitted Prior Art (figures 1-2) teaches an encapsulant (7). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate

an encapsulant of Admitted Prior Art into the device of Tay et al. because it protects device from the external environment. The combined device shows that an encapsulant for encapsulating the semiconductor chip and the added wire bonding units.

Regarding claim 15, the combined device inherently teaches a solder ball connected to the redundant solder ball pad (80).

Response to Arguments

Applicant's arguments with respect to claims 1-10, 12-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 703-305-3826. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

qv
June 30, 2003

Steven Loke
Primary Examiner